IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants: Carns et al.

Assignee: ZiLOG, Inc.

Title: "Process to Improve High Performance Capacitor Properties in Integrated MOS Technologies"

Appl. No.: 09/351,544 Filing Date: July 12, 1999

Examiner: Paul E. Brock II TC/Art Unit: 2815

Docket No.: ZIL-204

June 21, 2004

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APPEAL BRIEF

Dear Sir:

This Appeal Brief, filed in triplicate, is in support of the appeal noticed April 20, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, ZiLOG, Inc., as named in the caption above.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals and Interferences (the "Board") in the pending appeal.

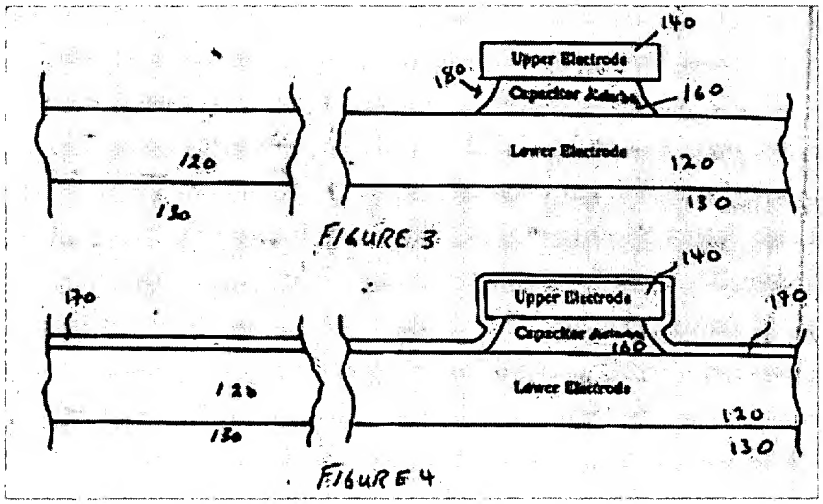
III. STATUS OF CLAIMS

The application at issue, filed on July 12, 1999, included 30 claims. In various amendments, claims 31-114 were added, and claims 1-2, 12-35, 40-71, 75-101 and 107-108 were cancelled. In a final Office Action dated January 20, 2004, the Examiner withdrew claims 109-114 due to the claims being drawn to a constructively elected invention. Appellants reserve the right to pursue claims 109-114 at a later time. Claims 3-11, 36-39, 72-74, 102-106 stand finally rejected and are the subject of this Appeal.

IV. STATUS OF AMENDMENTS

No amendments were made in the Response dated March 16, 2004 that was filed subsequent to the final Office Action dated January 20, 2004 (the "Final Office Action"). In an Amendment filed together with this Appeal Brief, claims 107-108 are cancelled, but no other changes are made.

V. SUMMARY OF INVENTION[1]



[1] The following summary pursuant to 37 CFR §1.192(a)(5) is a concise explanation of the claims and is to be read in light of the disclosure. This summary does not limit the claims. (See MPEP §1206)

A capacitor is formed in an integrated circuit by forming a lower electrode layer (120) on a semiconductor body (130), as shown in figure 3 of the above-captioned patent application. A dielectric layer (160) is formed over a portion of the lower electrode layer (120), and an upper electrode layer is formed over a portion of the dielectric layer (160). A portion of the upper electrode layer is removed to expose a portion of the dielectric layer, thereby forming an upper electrode (140) of a capacitor with a lateral boundary such that a portion of the dielectric layer is disposed in an inter-electrode region (180). The inter-electrode region (180) is within the lateral boundary of the upper electrode (140) and between the lower electrode layer (120) and the upper electrode (140).

A portion of the exposed portion of the dielectric layer is subsequently removed to expose a portion of the lower electrode layer, whereby a portion of the dielectric layer is removed from the inter-electrode region (180). Appellants' patent application states, "An unwanted consequence of step 10 is that, as discussed in the background section, some of the wanted dielectric is also removed. This is the undercutting indicated in Figure 3 at 180" (Application specification, page 10, lines 28-30). A conformal insulating layer (170), as shown in figure 4 of Appellants' application, is subsequently formed over a portion of the exposed portion of the lower electrode layer (120) proximate to the portion of the dielectric layer that is disposed within the inter-electrode region (180), thereby forming a portion of the conformal insulating layer (170) within the inter-electrode region. Then an anti-reflective layer (ARL) is formed over a portion of the conformal insulating layer (170) for use in a photolithographic process.

VI. ISSUES

The issues on appeal are:

1) Whether claims 3, 8-11, 36, 39, 72-74 and 102-105 are unpatentable under 35 U.S.C. §103 over Takahashi (USP 5,683,931) in view of Appellants' admitted prior art (AAPA) and in further view of Bencher et al.

("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109).

2) Whether the Examiner can force Appellants to label figures 2 and 3 as "Prior Art" and whether the Examiner has incorrectly characterized as "Applicant's admitted prior art (AAPA)" the Appellants' recognition that the undercutting is the source of a problem.

3) Whether claims 4-7, 37-38 and 106 are unpatentable under 35 U.S.C. §103 over Takahashi, the AAPA, and Bencher, in further view of Wang et al. (USP 5,545,585).

4) Whether claim 102 fails to meet the written description requirement under 35 U.S.C. §112, first paragraph, because the claim recites "using isotropic wet etching."

VII. GROUPING OF CLAIMS

Although claims 3-11, 36-39, 72-74 and 102-106 stand together, they do not fall together. Claims 3, 36 and 103 are independent claims of differing scope, each including subject matter distinct from one another. Each of claims 3, 36 and 103, however, recites a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Thus, each of the claims 3-11, 36-39, 72-74 and 102-106 contains the limitation of a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Claim 102 contains the additional limitation of using isotropic wet etching.

Claims 4-11, 74 and 102 depend on claim 3 and include limitations in addition to those of claim 3. Claims 37-39 depend on claim 36 and include limitations in addition to those of claim 36. Claim 73 depends on claim 72 and

includes a limitation in addition to those of claim 72. Claims 104-106 depend on claim 103 and include limitations in addition to those of claim 103.

VIII. ARGUMENT

A. Claims 3, 8-11, 36, 39, 72-74 and 102-105 (Issue No. 1)

The Examiner rejects claims 3, 8-11, 36, 39, 72-74 and 102-105 under 35 U.S.C. §103 for being rendered obvious over a three-way combination of Takahashi (USP 5,683,931), what the Examiner calls Applicant's admitted prior art (AAPA), and Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109). The Examiner states:

> "With regard to claim 3, Takahashi discloses in figures 2a-2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a lower electrode (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305) over a portion of the lower electrode. Takahashi discloses in figure 2b forming a upper electrode layer (306) over a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the upper electrode layer to expose a portion of the dielectric layer, thereby forming an upper electrode with a lateral boundary, wherein a portion of the dielectric layer is disposed in an inter-electrode region, the inter-electrode region disposed within the lateral boundary of the upper electrode and between the lower electrode layer and the upper electrode. Takahashi discloses in figure 2c subsequently removing a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode layer. Takahashi is silent to wherein a portion of the dielectric layer is removed from the inter-electrode region. Takahashi is silent to a method of etching this process step." (Final Office Action, p. 4, line 21 – p. 5, line 10)

In an attempt to remedy Takahashi's failure to disclose removing dielectric material from an inter-electrode region, the Examiner cites what he calls "Applicant's Admitted Prior Art (AAPA)". The Examiner states, "The AAPA teaches in figure 2, figure 3, page 3, lines 11 and 12, page 4, line 25 – page 5, line 2, and page 10, lines 20-30 a method of etching a capacitor dielectric layer (60/160) wherein a portion of the dielectric layer is removed from an inter-electrode region (180)" (Final Office Action, p. 5, lines 10-20). The Examiner then asserts:

> "It would have been obvious to one of ordinary skill in the art to use the etching step resulting in removing a portion of the dielectric layer in an inter-electrode region of the AAPA in the method of Takahashi in order to perform the etching step suggested, but not defined, in column 2, lines 20-23, of Takahashi using a process well known as suggested by the cited sections of the AAPA. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over a portion of the exposed portion of the lower electrode layer proximate to the portion of the dielectric layer disposed in the inter-electrode region. It would have been further obvious in the method of Takahashi and the AAPA whereby a portion of the conformal insulating layer is formed in the inter-electrode region. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer." (Final Office Action, p. 5, line 13 – p. 6, line 1)

The Examiner then admits that the hypothetical Takahashi/AAPA combination fails to include an anti-reflective layer. The Examiner states, "Takahashi and AAPA are silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer" (Final Office Action, p. 6,

lines 1-2). The Examiner therefore cites another reference, the Bencher patent, and states:

> "Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi and the AAPA in order to improve the photolithographic mask in the method of Takahashi and the AAPA in order to improve the photolithographic process by reducing net linewidth variations as stated by the AAPA on page 1, lines 14-15 of the originally filed specification. (Final Office Action, p. 6, lines 2-9)

Appellants' Response

The Examiner rejects claims 3, 8-11, 36, 39, 72-74 and 102-105 under 35 U.S.C. §103 as being obvious over a three-way combination of Takahashi, Bencher and the AAPA. The Examiner's rejection should be withdrawn because the Examiner improperly characterized the AAPA as prior art, and neither Takahashi nor Bencher discloses a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Moreover, the Examiner has not identified a motivation to combine Takahashi with the AAPA and then a motivation to combine the combination Takahashi/AAPA with Bencher.

i. The AAPA is not prior art (Issue No. 2).

The Examiner labels as prior art various teachings of the Appellants' patent application that relate to removing a dielectric layer from an inter-electrode

region or undercutting, including "figure 2, figure 3, page 3, lines 11 and 12, page 4, line 25 – page 5, line 2, and page 10, lines 20-30" (Final Office Action, p. 5, lines 10-11). Moreover, the Examiner states that "Figures 2 and 3 should be designated by a legend such as –Prior Art— . . . A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application" (Final Office Action, page 3, lines 6-8).

The teachings in Appellants' application specification of (a) the existence of undercutting in an inter-electrode region, and (b) a problem associated with undercutting when the structure is covered by an anti-reflective layer (ARL) do not appear in a section of Appellants' specification entitled "PRIOR ART." Instead, the section is called "Background of the Invention." Appellants' patent application states, "Figure 2 shows an embodiment of the present invention at the state where the upper electrode has been defined. Figure 3 shows the same embodiment after the excess capacitor dielectric has been removed" (Application specification, page 7, lines 26-29). Appellants' patent application also states, "An unwanted consequence of step 10 is that ... some of the wanted dielectric is also removed. This is the undercutting indicated in Figure 3 at 180" (Application specification, page 10, lines 28-30). Appellants state for the record that the problem they have identified is not prior art. Figures 2 and 3 were not designated by a legend such as "Prior Art" because they do not depict prior art but rather the source of a problem identified by Appellants and solved by the invention.

The Examiner does not contend that either Takahashi or Bencher discloses the limitation of a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. "Takahashi is silent to wherein a portion of the dielectric layer is removed from the inter-electrode region" (Final Office Action, p. 5, lines 8-9). "Bencher teaches . . . forming an anti-reflective layer (ARL) . . ." (Final Office Action, p. 6, lines 2-4). Therefore, no combination of Takahashi and Bencher without the AAPA could have resulted in Appellants' invention in those claims that recite a conformal insulating layer filled, provided or

formed in an inter-electrode region or in an undercutting. Thus, the invention of claims 3-11, 36-39, 72-74, 102-106 is unobvious over the prior art because the prior art does not describe the limitation of a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting, and all of the claims 3-11, 36-39, 72-74, 102-106 contain that limitation.

ii. No motivation to combine Takahashi and AAPA and Bencher.

Moreover, even if the AAPA were found to be prior art, the Examiner has not identified a motivation or suggestion to combine Takahashi with the AAPA and with Bencher. The Examiner identifies only a motivation "to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask . . . in order to improve the photolithographic process by reducing net linewidth variations . . ." (Final Office Action, p. 6, lines 6-8). The motivation identified by the Examiner is not a motivation to combine Takahashi with the AAPA and with Bencher, but rather is only a motivation to combine Bencher with references that seek to solve the problem of excessive variation in net linewidths. One of ordinary skill in the art, who was confronted with the problem of capacitor leakage, would not have been motivated by to combine Takahashi with the AAPA and with Bencher where reducing net linewidth variation was not a primary consideration.

The Examiner argues "that if a solution to a different problem than that confronted by the applicant is solved, motivation exists for the combination. In this case, reduced linewidth variation will improve the device performance. Motivation can exist independently of the reason applicant was motivated to make the present invention" (Final Office Action, p. 14, lines 2-5). Admittedly, the Federal Circuit has held that "[a]s long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor." In re Beattie, 974 F.2d 1309, 1312, 24 USPQ2d 1040, 1042

(Fed. Cir. 1992). See also In re Dillon, 919 F.2d 688, 693, 16 USPQ2d 1879, 1901 (Fed. Cir. 1990), cert. denied., 500 U.S. 904 (1991).

In this case, however, the invention includes the discovery of the source of a problem, namely that the existence of undercutting increases leakage current in capacitors when they are covered by anti-reflective layers. "[W]here the claimed invention solves a problem, the discovery of the source of the problem and its solution are considered to be part of the 'invention as a whole' under 35 U.S.C. 103." Ex parte Hiyamizu, 10 USPQ2d 1393, 1394-5, (Bd.Pat.App & Interf. Apr 28, 1998), citing In re Kaslow, 707 F.2d 1366, 217 USPQ 1089 (Fed. Cir. 1983) and In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1979) ("[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified.") Moreover, "[d]efining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness." Monarch Knitting Mach. Corp. V. Sulzer Morat GmbH, 139 F.3d 877, 880, 45 USPQ2d 1977, 1981 (Fed. Cir. 1998). See also Ecolochem Inc. V. Southern California Edison, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000).

In the present case, it is not pertinent whether the combination of Takahashi, the AAPA and Bencher also has the attribute of solving another problem not confronted by the inventors. There still must be evidence that a "skilled artisan, confronted with the same problem as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." In re Rouffet, 149 F.3d 1350, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998). One of ordinary skill in the art would not have been motivated to combine Bencher with Takahashi and the AAPA to solve the problem of current leaking through an anti-reflective layer from one capacitor plate to another. One of ordinary skill in the art would not have been inclined to use the teaching of Bencher (which discloses an anti-reflective layer) to solve the identified problem because the identified problem does not occur unless an anti-reflective layer is used. The Examiner admits that

"Takahashi and the AAPA are silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer" (Final Office Action, p. 6, lines 1-2). So the identified problem that results from an antireflective layer would not have presented itself to one of ordinary skill in the art who was in possession of the teachings of Takahashi and the AAPA. It is improper for the Examiner to consider a motivation resulting from a different problem where the different problem would not have arisen but for the very invention disclosed by the Appellants.

Therefore, the §103 rejection of claims 3, 8-11, 36, 39, 72-74 and 102-105 as being unpatentable under 35 U.S.C. §103 over Takahashi in view of the AAPA and in further view of Bencher should be withdrawn. Appellants respectfully submit that these claims are allowable.

B. Claims 4-7, 37-38 and 106 (Issue No. 3)

The Examiner rejects claims 4-7, 37-38 and 106 under 35 U.S.C. §103 for being rendered obvious over a four-way combination of Takahashi, the AAPA, Bencher and Wang et al. (USP 5,545,585).

Claims 4-7 depend directly or indirectly from claim 3. Dependent claims 4-7 are therefore allowable for at least the same reasons explained above for which claim 3 is allowable. Claims 37-38 depend directly from claim 36. Claims 37-38 are therefore allowable for at least the same reasons explained above for which claim 36 is allowable. Claim 106 depends directly on claim 103 and is, therefore, allowable for at least the same reasons explained above for which claim 103 is allowable.

C. Claim 102 (Issue No. 4)

The Examiner rejects claim 102 under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement. The Examiner states, "It is not clear where in the originally filed specification support for 'using isotropic

wet etching' can be found" (Final Office Action, page 3, line 19 - page 4, line 2). Claim 3 recites, " . . . step (e) is performed using isotropic wet etching."

In rejecting claim 102 under §112, first paragraph, the Examiner is arguing that new matter has been added in the claims by the use of the term "isotropic wet etching." New matter has not been added simply because a claim term does not appear in the specification. In this case, the concept of isotropic wet etching was described in the originally-filed specification "in such full, clear, concise and exact terms as to enable any person skilled in the art" to make and use the invention. 37 C.F.R. §1.71. The specification describes a step that involves isotropic wet etching. The specification discloses:

> "Step 10 is the etch of the capacitor dielectric. In the preferred embodiment, this is a Buffered Oxide Etch (BOE), although other embodiments could employ a dry or other etch. ... The result of this process is shown in Figure 3. ... An unwanted consequence of step 10 is that ... some of the wanted dielectric is also removed. This is the undercutting indicated in Figure 3 at 180" (Application specification, page 10, lines 20-30).

Isotropic means "of equal physical properties along all axes." Random House Webster's Unabridged Dictionary, Second Edition, 1997. Anisotropic etching results in vertical walls, whereas isotropic etching also etches in the horizontal direction. The mention of "undercutting", and its illustration as reference character 180 in figure 3, is a disclosure that the etching of step 10 is isotropic. In addition, the specification states that although one embodiment employs a Buffered Oxide Etch, a dry or other etch can also be used. One of ordinary skill in the art would have known that a Buffered Oxide Etch is a wet etch, as opposed to a dry or other etch. If the Board so requests, Appellants will produce an affidavit stating that one of ordinary skill in the art would have known that a Buffered Oxide Etch is a wet etch. Therefore, the specification discloses

isotropic wet etching, and the §112, first paragraph, rejection should be withdrawn.

VIII. CONCLUSION

Each of the claims 3-11, 36-39, 72-74, 102-106 recites a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. This structural feature is not disclosed in any reference cited by the Examiner, other than in Appellants' application specification. The disclosure of this feature in Appellants' application specification does not render the disclosure "prior art." The discovery that undercutting is a source of the problem of current leaking through an anti-reflective layer from one capacitor plate to another is part of Appellants' invention. The source of the problem identified by Appellants is nowhere recognized in the cited prior art. Therefore, Appellants' own disclosure of the problem and its source cannot properly be used as one of the references in a three-way obviousness rejection. Moreover, the references cited by the Examiner do not contain a motivation or suggestion to combine either (i) the three references that are the basis for the rejection of claims 3, 8-11, 36, 39, 72-74 and 102-105 or (ii) the four references that are the basis for the rejection of claims 4-7, 37-38 and 106. Therefore, Appellants respectfully request that the Board reverse the rejections of pending claims 3-11, 36-39, 72-74 and 102-106.

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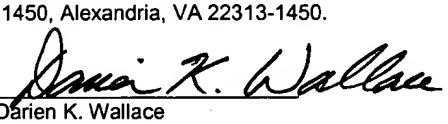
By 
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Date of Deposit: June 21, 2004

Respectfully submitted,

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IX. APPENDIX

Claims 1 – 2 (canceled)

3. (previously presented): A method of forming a capacitor in an integrated circuit comprising:

(a) forming a lower electrode layer on a semiconductor body;

(b) forming a dielectric layer over a portion of said lower electrode layer;

(c) forming an upper electrode layer over a portion of said dielectric layer;

(d) removing a portion of said upper electrode layer to expose a portion of said dielectric layer, thereby forming an upper electrode with a lateral boundary, wherein a portion of said dielectric layer is disposed in an inter-electrode region, said inter-electrode region disposed within said lateral boundary of said upper electrode and between said lower electrode layer and said upper electrode;

(e) subsequently removing a portion of said exposed portion of said dielectric layer to expose a portion of said lower electrode layer, wherein a portion of said dielectric layer is removed from said inter-electrode region;

(f) subsequently forming a conformal insulating layer over a portion of said exposed portion of said lower electrode layer proximate to said portion of said dielectric layer disposed in said inter-electrode region, whereby a portion of conformal insulating layer is formed in said inter-electrode region; and

(g) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal insulating layer.

4. (previously presented): The method of claim 3, wherein said conformal insulating layer has a thickness ranging from 20 angstroms to 70 angstroms.

5. (previously presented): The method of claim 3, wherein said conformal insulating layer is an oxide layer formed in a thermal process.

6. (previously presented): The method of claim 5, wherein said thermal process is a rapid thermal oxidation (RTO) performed for a length of time ranging from 10 to 60 seconds and at a temperature ranging from 850°C to 1050°C.

7. (previously presented): The method of claim 3, wherein said conformal insulating layer is formed by deposition.

8. (original): The method of claim 3, wherein said ARL is an anti-reflective coating.

9. (original): The method of claim 3, wherein said ARL is titanium nitride.

10. (original): The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. (previously presented): The method of claim 10, wherein said plasma enhanced chemical vapor deposition anti-reflective layer (PEARL) has a thickness ranging from 300 angstroms to 400 angstroms.

Claims 12 – 35 (canceled)

36. (previously presented): A method of forming an integrated circuit comprising:

(a) forming a conductive layer on a semiconductor body;

(b) forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer, wherein said top electrode has a lateral boundary; and

a dielectric layer between said top electrode and said conductive layer;

(c) forming a conformal insulating layer over said capacitor structure and a portion of said conductive layer proximate to said capacitor structure, wherein a portion of said conformal insulating layer is formed in an inter-electrode region

within said lateral boundary of said top electrode and between said top electrode and said conductive layer;

(d) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal layer;

(e) forming a patterned mask over said anti-reflective layer (ARL); and

(f) etching said conductive layer using said patterned mask.

37. (previously presented): The method of claim 36, wherein said conformal insulating layer has a thickness ranging from 20 angstroms to 70 angstroms.

38. (previously presented): The method of claim 36, wherein said conformal insulating layer is an oxide layer formed in a thermal process.

39. (previously presented): The method of claim 36, wherein said conductive layer is additionally used to form a gate of one or more transistors formed on said integrated circuit.

Claims 40 – 71 (canceled)

72. (previously presented): The method of claim 3, further comprising:

(h) forming a photoresist mask over a portion of said anti-reflective layer (ARL); and

(i) irradiating said photoresist mask with radiation that penetrates said photoresist mask, wherein said anti-reflective layer reduces a reflection of said radiation by 70% or more.

73. (previously presented): The method of claim 72, wherein the anti-reflective layer reduces said reflection of said radiation by 70% to 85%.

74. (previously presented): The method of claim 3, wherein said anti-reflective layer is a Si_xON_y film.

Claims 75 – 101 (canceled)

102. (previously presented): The method of claim 3, wherein said subsequently removing a portion of said exposed portion of said dielectric layer in step (e) is performed using isotropic wet etching.

103. (previously presented): A method comprising:

(a) forming a lower electrode layer upon an underlying layer of a semiconductor device;

(b) forming a capacitor dielectric layer;

(c) forming an upper electrode layer, wherein said capacitor dielectric layer is disposed in an inter-electrode region between said lower electrode layer and said upper electrode layer;

(d) removing a portion of said upper electrode layer such that an upper electrode is formed having an edge;

(e) removing a portion of said dielectric layer such that an exposed portion of said lower electrode layer is formed and such that an undercutting is formed in said inter-electrode region underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting;

(f) providing a conformal insulating layer over said upper electrode and over said exposed portion of said lower electrode layer such that said undercutting is filled in by said conformal insulating layer; and

(g) providing a anti-reflective layer over said conformal insulating layer.

104. (previously presented): The method of claim 103, wherein the forming in step (b) is performed by depositing said capacitor dielectric layer to a thickness ranging from 300 angstroms to 800 angstroms.

105. (previously presented): The method of claim 103, wherein said underlying layer electrically isolates said lower electrode layer.

106. (previously presented): The method of claim 103, wherein the providing the conformal insulating layer in step (f) is performed using a rapid thermal oxidation (RTO) process to grow a layer of silicon oxide to a thickness ranging from 20 angstroms to 100 angstroms.

Claims 107 – 108 (canceled)

109. (withdrawn): A device comprising:

a lower electrode layer disposed on an underlying layer of a semiconductor substrate;

a capacitor dielectric disposed on said lower electrode layer;

an upper electrode disposed on said capacitor dielectric, wherein said upper electrode has a lateral boundary, wherein said capacitor dielectric is disposed within an inter-electrode region, said inter-electrode region disposed within said lateral boundary between said lower electrode layer and said upper electrode layer, and wherein an exposed portion of said lower electrode layer lies outside said lateral boundary;

a conformal layer of an insulating material disposed over said upper electrode and over said exposed portion of said lower electrode layer;

an undercutting in said inter-electrode region, wherein said capacitor dielectric is absent from said undercutting and said undercutting is filled by said insulating material; and

an anti-reflective layer disposed over said conformal layer of said insulating material.

110. (withdrawn): The device of claim 109, wherein said anti-reflective layer is titanium nitride.

111. (withdrawn): The device of claim 109, wherein said anti-reflective layer is a plasma enhanced anti-reflective layer (PEARL).

112. (withdrawn): The device of claim 109, wherein said lower electrode layer is polysilicon.

113. (withdrawn): A device comprising:

a lower electrode layer disposed on an underlying layer of a semiconductor substrate;

a capacitor dielectric disposed on said lower electrode layer;

an upper electrode disposed on said capacitor dielectric, wherein said upper electrode has a lateral boundary, wherein said capacitor dielectric is disposed in an inter-electrode region, said inter-electrode region disposed within said lateral boundary and between said lower electrode layer and said upper electrode layer, and wherein an exposed portion of said lower electrode layer lies outside said lateral boundary;

an anti-reflective layer disposed over said upper electrode and over said exposed portion of said lower electrode layer; and

means for preventing an electrical connection through said anti-reflective layer from said upper electrode to said lower electrode layer, wherein said means is at least partially disposed within said inter-electrode region.

114. (withdrawn): The device of claim 113, wherein said anti-reflective layer is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).